UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/989,563	11/19/2001	Joseph C. Sher	MICRON.113C1	2553

20995 7590 05/31/2002

KNOBBE MARTENS OLSON & BEAR LLP
620 NEWPORT CENTER DRIVE
SIXTEENTH FLOOR
NEWPORT BEACH, CA 92660

EXAMINER
TRA, ANH QUAN

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 05/31/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/989,563	SHER ET AL.	
	Examiner	Art Unit	
	Quan Tra	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *4/19/2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

This office action is in response to the amendment filed 4/19/2002. The rejection under 35 U.S.C. 103(a) in previous office action is maintained.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Javaniferd et al. (USP 5483486, Applicant submitted IDS) in view of Furumochi (USP 5473277, Applicant submitted IDS).

As to claim 1, Javanifrad et al. shows in figure 14 a circuit comprising: a reference circuit (316); a voltage regulator (318) electrically coupled to the reference circuit which generates a first control signal (REG); a charge pump (320) which receives the control signal from the voltage regulator, the charge pump generating the test supply voltage (Vout). Thus, figure 14 shows all limitations of the claim except for the reference having a plurality of voltage regulation devices and at least one bypass device connected to at least one of the plurality of voltage regulation devices. However, Furumochi's figure 5 shows a reference circuit having plurality of voltage regulation devices (T1-T4) and at least one bypass device (SW0) connected to at least one of the plurality of voltage regulation devices. Furumochi's circuit having the advantage of varying the voltage level at the output node (OUT). Thus, it would have been obvious to one having ordinary skill in the art to use Furumochi's figure for Javanifrad et al.'s reference circuit

for the purpose of generating a variable reference voltage, therefore controlling the output level of the charge pump. Thus, with the combination, it is inherent that the at least one bypass device (SWO(TN4)) is activated following the certification of the semiconductor device to bypass the at least one of the plurality of voltage regulation devices from the clamp circuit to lower the clamping threshold of the clamp circuit, the voltage regulator generating a second control signal responsive to the lowered clamping threshold of the clamp circuit to cause the charge pump to generate the operational supply voltage.

As to claim 2, Furumochi's figure 5 shows the plurality of voltage regulation devices comprise diodes.

As to claim 3, Furumochi's figure 5 shows the diodes are implemented through transistors.

As to claim 4, Furumochi's figure 5 further shows the bypass device comprising a fuse (FU) in series with a transistor (TN4).

As to claim 5, Furumochi's figure 5 shows bypass device is activated by blowing the fuse.

As to claim 6, with the combination of the prior arts, it is inherent that value of the operational supply voltage is reduced for each voltage regulation device bypassed.

As to claim 7, with the combination of the prior arts, it is inherent that the voltage regulation devices limit the maximum voltage output of the clamp circuit.

As to claim 8, with the combination of the prior arts, it is inherent that the first control signal reduces the test supply voltage when the voltage regulation devices limit the output of the clamp circuit.

As to claim 9, with the combination of the prior arts, it is inherent that the second control signal reduces the operational supply voltage when the non-bypassed voltage regulation devices (T1, T2..) limit the output of the clamp circuit.

Claims 10-21 and 25 recite similar limitations of claims 1-9. Therefore, they are rejected for the same reasons (see further in figure 4).

As to claim 22, the prior art fails to shows the step of reversibly (by blowing fuse FU) bypassing at least one of the plurality of voltage control elements; establishing a third voltage control signal during a third period from the plurality of voltage control elements which are not reversibly bypassed; and generating a third supply voltage from the third voltage control signal. However, it is seen as an design choice and obvious to one having ordinary skill in the art to bypass Furumochi's another diode for the purpose of further reducing the output voltage level (OUT).

As to claim 23, Furumochi's figure 5 shows reversibly bypassing at least one of the plurality of voltage control elements comprises blowing a fuse.

As to claim 24, it is seen as an obvious design choice for reversibly bypassed the diode after testing of the semiconductor device dependent upon particular environment of use to ensure optimum performance.

Response to Arguments

Applicant's arguments have been fully considered but they are not persuasive. In response to the arguments of the last fourth lines in page 4 to the end of second paragraph in page 5, it is well known that diode works as a clamp. The diodes in Furumochi's circuits forcing the output node to a fix voltage. Therefore, Furumochi's reference circuit can be considered as clamp

circuits. Applicant states that "In column 7 at lines 15-17, Furmochi states that figure 5 shows a constant voltage renerator circuit for ...Furumochi does not teach or suggest that the input voltage Vcc ever decreases in magnitude". Nowhere in the claims recited that Vcc decreases in magnitude. Furthermore, it is seen as inherent for the supply voltage to be vary. That why the diodes is used in the circuit for the purpose of generating a fix reference voltage when the supply voltage exceed the threshold voltages of the diodes.

In response to the arguments of the last 9 lines in page 5 to the first three lines in page 6. Applicant states that "Furumochi shows two transistors T4 and TN4, both which are n-type field effect transistors having the same voltage drop from the source to the drain. Therefore, transistor TN4 does not lower the claim threshold of the clamp circuit". The Examiner respectfully disagrees. Transistors T4 and TN4 having different gate-source voltages. Therefore, they have different source to drain voltage drop. Nowhere in column 7, lines 23-25 and 45-46 recite that "transistors T4 and TN4 having the same voltage drop from the source to the drain". Thus, when transistor TN4 is turned on, output voltage (out) will be lower than the previous voltage.

The same response for the arguments of claim 10, in page 6.

In response for the arguments of claim 17, (page 6 to page 7), Furumochi's figure 4 shows the step of generating the first supply voltage (Vout when switch 11A opened) from the first control signal and reversibly bypassing at least one of the plurality of the voltage control elements (by switch 11A) which are not reversibly bypass, a second supply voltage (Vout when switch 11a closed) from the second control signal. Thus, Furomochi shows all limitations of the claim.

Conclusion

3. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. These references are cited as interest because they show some circuits analogous to the claimed invention.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quan Tra whose telephone number is 703-308-6174. The examiner can normally be reached on 8:00 A.M.-5:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 703-308-4876. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

QT
May 20, 2002

Terry D. Cunningham
Primary Examiner